AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (currently amended) A semiconductor integrated circuit comprising:

a combination circuit~~,~~; and

a scan diagnosis circuit capable of performing a scan test of said combination circuit;

wherein

said scan diagnosis circuit comprises:

a first scan chain having a plurality of scan flip-flops connected for operating in synchronization with a clock signal;

a second scan chain placed behind said first scan chain, and having a plurality of scan flip-flops connected for operating in synchronization with the clock signal;

a first clock buffer for supplying the clock signal in the direction opposite to the flow direction of scan test data that passes through said first scan chain;

a second clock buffer for supplying the clock signal in the direction opposite to the flow direction of scan test data that passes through said second scan chain;

and

a return path for sending scan test data output from a scan flip-flop placed at a closest position to said first clock buffer in said first scan chain to a scan flip-flop placed at a furthermost position from said second clock buffer in said second scan chain.

2. (previously presented) A semiconductor integrated circuit according to claim 1, wherein

said return path is formed of a wiring finer than a wiring forming a feeder line of said clock signal.

3. (previously presented) A semiconductor integrated circuit according to claim 1, wherein

the circuit has multilayered wirings with a resistance per unit length differing between layers, and said return path is formed of a wiring having higher resistance than a wiring forming a feeder line of said clock signal.

4. (previously presented) A semiconductor integrated circuit according to claim 1, wherein

an area for inserting delay elements on the scan test data path in said return path is predefined to insert said delay elements in the area.

5. (currently amended) A semiconductor integrated circuit according to claim 1, further comprising:

a third clock buffer for scan test, capable of delaying the output signal of said first clock buffer; and

a selector, capable of supplying the output signal of said third clock buffer instead of the output from said first clock buffer at the time of scan test to said first scan chain.

Claim 6 (cancelled)

7. (currently amended) A semiconductor integrated circuit comprising:

a combination circuit; and

a scan diagnosis circuit capable of performing a scan test of said combination circuit;

said scan diagnosis circuit comprising:

a plurality of first flip-flops having first clock signal line connected;

a plurality of second flip-flops having second clock signal line connected;

a first clock buffer connected to said first clock signal line; and

a second clock buffer connected to said second

clock signal line;

wherein

said first clock buffer supplies a first clock signal to said first clock signal line;

said second clock buffer supplies a second clock signal to said second clock signal line;

said plurality of first flip-flops is formed on a first virtual line extending in a first direction, having data transferred from one end to the other end of said plurality of first flip-flops at the time of scan test;

said plurality of second flip-flops is formed on a second virtual line, which is in parallel to said first virtual line, having data from one end to the other end of said plurality of second flip-flops at the time of scan test;

data output from the other end of said plurality of first flip-flops is input to the one end of said plurality of second flip-flops;

said first clock buffer is configured such that the distance from said first clock buffer to the other end of said plurality of first flip-flops is shorter than the distance from said first clock buffer to the one end of said plurality of first flip-flops; and

said second clock buffer is configured such that the

distance from said second clock buffer to the other end of said plurality of second flip-flops is shorter than the distance from said second clock buffer to the one end of said plurality of second flip-flops.

8. (previously presented) A semiconductor integrated circuit according to claim 7, further comprising:

a third clock buffer for supplying a common clock signal to said first clock buffer and said second clock buffer.

9. (previously presented) A semiconductor integrated circuit according to claim 7, wherein

a resistance of a wiring for connecting the other end of said plurality of first flip-flops with the one end of said plurality of second flip-flops is greater than a resistance of a first clock signal wiring and of a second clock signal wiring.

10. (previously presented) A semiconductor integrated circuit according to claim 9, wherein

a wiring connecting the other end of said plurality of first flip-flops with the one end of said plurality of second flip-flops is finer than said first clock signal

wiring and said second clock signal wiring.

11. (previously presented) A semiconductor integrated circuit according to claim 7, wherein

said combination circuit is disposed between said plurality of first flip-flops and said plurality of second flip-flops.

12. (currently amended) A semiconductor integrated circuit according to claim 7, further comprising:

a fourth clock buffer connected to said second clock buffer~~,~~; and

a selector for selecting one of a path for supplying said second clock signal directly from said second clock buffer to said plurality of second flip-flops or a path for supplying said second clock signal through said second and fourth clock buffers to said plurality of second flip-flops.

13. (previously presented) A semiconductor integrated circuit according to claim 2, wherein

an area for inserting delay elements on a scan test data path in said return path is predefined to insert said delay elements in the area.

14. (previously presented) A semiconductor integrated circuit according to claim 3, wherein

an area for inserting delay elements on a scan test data path in said return path is predefined to insert said delay elements in the area.

15. (currently amended) A semiconductor integrated circuit according to claim 2, further comprising:

a third clock buffer for scan test, capable of delaying the output of the clock signal of said first clock buffer; and

a selector, capable of supplying the clock signal of said third clock buffer instead of the clock signal from said first clock buffer at the time of scan test to said first scan chain.

16. (currently amended) A semiconductor integrated circuit according to claim 3, further comprising:

a third clock buffer for scan test, capable of delaying the output of the clock signal of said first clock buffer; and

a selector, capable of supplying the clock signal of said third clock buffer instead of the clock signal from said first clock buffer at the time of scan test to said

first scan chain.

17. (currently amended) A semiconductor integrated circuit according to claim 4, further comprising:

a third clock buffer for scan test, capable of delaying the output of the clock signal of said first clock buffer; and

a selector, capable of supplying the clock signal of said third clock buffer instead of the clock signal from said first clock buffer at the time of scan test to said first scan chain.